REMARKS

This paper amends Claims 1, 7 and 13 to emphasize that the first, second and third photoresist layers are the first, second and third **color** photoresist layers, in order to more clearly distinguish the claimed invention from the cited references. Claim 1 is also amended to emphasize that the substrate is a substrate of a **flat panel display**. Support for the amendments can be found on pages 4-8 of the specification.

At pages 4-6 of the final Office Action dated October 21, 2003, the Examiner rejects claims 1, 4, 7, 10, 13 and 16 under 35 USC 103(a) as being unpatentable over Suzuki et al. (US Patent No. 6,043,145) in view of Kurauchi et al. (US Patent No. 6,323,921). Moreover, at pages 6-7, claims 2, 3, 5, 6, 8, 9, 11, 14, 15, 17 and 18 are rejected under 35 USC 103(a) as being unpatentable over Suzuki et al. and Kurauchi et al. in further view of Lin et al. (US Patent No. 6,063,653). These rejections are respectfully traversed. The Applicant has addressed the cited references in the response dated July 21, 2003. This time, the Applicant's comments mainly respond to the Examiner's arguments at pages 2-4 of the final Office Action ("Response to Arguments").

In section I, the Examiner argues that Suzuki et al. is reasonably pertinent to the particular problem with which the application is concerned, because Applicant is essentially claiming a method of forming through holes in resist layers. The Applicant respectfully disagrees. It is highly unlikely that a person having ordinary skill in the art of flat panel display (the technical area of the present application) would use any features from Suzuki et al. (relating to multilayer wiring structure). Suzuki et al. concerns neither color filter nor thin film transistors, not to mention forming both on the same substrate of a flat panel display. For a person working on a flat display panel, it takes an inventive step to incorporate features from a reference regarding multilayer wiring structure.

Moreover, the Applicant respectfully submits that it would not have been obvious to combine Suzuki et al. with Kuranchi et al. (as suggested by the Examiner in section V). Suzuki et al. relates to a method for fabricating a multilayer wiring structure of a semiconductor integrated circuit, and Kurauchi et al. relates to a color filter substrate and a LCD device, which are not even in proximate technology fields. A semiconductor engineer would have no reason to search and study references regarding LCD devices, nor vice versa.

In section V, the Examiner asserts that one of ordinary skill in the art at the time the invention was made would have had a reason, suggestion and motivation to combine the teachings of Kurauchi with that of Suzuki (or to take Kurauchi alone) for a multi-layer structure having the recited elements of independent claims at least for a high opening ratio as specifically taught in Kurauchi. However, the aspect ratio, regarded as the opening ratio as the Examiner implies, disclosed by Suzuki in fact means size of a connecting hole in diameter and in depth (see column 2 lines 42-47, and column 5 lines 7-12), and the connecting hole in 0.25 μm generation is approximately 0.35 μm in diameter and approximately 0.6 μm in depth and in 0.18 μm generation is approximately 0.20 μm in diameter and approximately 3 in aspect ratio. The opening ratio (also referred as to the aperture ratio) disclosed by Kurauchi, on the other hand, refers to the relationship between the pixel region and the non-pixel region. For example, if the spacer portions are disposed in the non-pixel region, such as on the wiring such as scanning lines, the opening ratio becomes high (see column 1 lines 36-46 and column 4 lines 48-51).

In section III, the Examiner asserts that in Suzuki et al., a resist is used to etch contact holes through the insulating layers and implies that such resist reads on the photoresist layers recited by claim 1. The Applicant respectfully disagrees. First, a resist is not equivalent of a photoresist layer. Second, the cited references fail to disclose **three** separate photoresist layers, which covers **three** separate groups of the pixels. The Examiner does not respond to the argument that Suzuki et al. does not mention "a plurality of pixels" and that the first, second and third photoresist layers cover three different groups of the pixels.

In section IV, the Examiner asserts that Kuranchi et al. disclose a structure in which both the color filter and the black matrix are formed on the TFT array substrate. Note that in Kuranchi et al., the color photoresist layers are spacer portions (9a, 9b and 9c) provided on the light shielding films (4a, 4b and 4c) or the scanning line (25) (see column 5 lines 34-44, column 6 lines 55-58, column 8 lines 48-49, Figs. 1-3, Fig. 4A, and Figs. 5A-5C). Therefore, Kurauchi fails to disclose, teach or suggest "wherein **the first area** (where switching units are formed) of each pixel is covered by at least two of the first, second and third color photoresist layers" recited in Claim 1 of the present application.

Due to the reasons stated above, the Applicant believes that independent Claims 1, 7 and 13 are patentable over the cited references. Claims 2-6, 8-12 and 14-18 are also patentable, at least by virtue of their dependency from Claims 1, 7 or 13.

The Applicant has attempted to address all of the issues raised by the Examiner in the Office Action as the Applicant understands them. The Applicant believes that the Application is now in condition for allowance. If any point requires further explanation, the Examiner is invited to telephone Troy Cai at (323) 934-2300 or e-mail Troy Cai at tcai@ladasparry.com.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (703)872-9306 on

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(Date of Deposit)

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3/29/04

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